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EXAMINER	
MOORE, PATRICK M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,960	PETERSEN ET AL.	
	Examiner	Art Unit	
	Patrick M. Moore	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-68 have been examined.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 30-42 & 61-68 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding **Claims 30-42:** As claimed, "a global arbiter" lacks sufficient limitation requiring a hardware structure necessary for any functionality to be realized, which is required by Sec. 101. As defined by **¶0016** of Applicant's specification, a global arbiter is a computer program product, which Examiner understands to be software, per se. As claimed, the global arbiter could be nothing more than non-functional descriptive material. As further set forth in MPEP 2106, a claim directed towards functional descriptive material should "be recorded on some computer-readable medium [to] become structurally and functionally interrelated to the medium". Examiner notes that further limiting the global arbiter to be executed on computer readable medium would, most likely, direct Claims 30-42 to statutory subject matter.

b. Regarding **Claims 61-68:** As defined on page 30 of Applicant's Specification, a transmission medium and a computer usable medium, which both include carrier waves, constitutes non-statutory subject matter. A signal, as claimed by applicant, does not fall within any of the patent eligible categories set

forth by 35 U.S.C. 101: process, machine, manufacture or composition of matter. As set forth in 1 Chisum, Sec. 1.02[3] (citing W. Robinson, The Law of Patents for Useful Inventions 270 (1890)), a product is a tangible physical article or object, some form of matter, which a signal is not. That the other product classes require physical matter is evidence that a manufacture was also intended to require physical matter. A signal or carrier wave, as a form of energy, does not fall within the definition of process, machine, manufacture or composition and therefore does not fall within one of the four statutory classes of Sec. 101

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-41, 43-48 & 50-68 are rejected under 35 U.S.C. 102(b) as being anticipated by Carpenter et al. (US Patent # 6,067,611), herein Carpenter.

a. **As per Claim 1,** Carpenter discloses a system-on-a-chip (SOC) having a plurality of agents which share a memory **[Column 3, Lines 38-48]**, the SOC comprising: a first bus interface **[Figure 1, #20]** coupled to a first one of the plurality of agents **[Figure 1, #10a]** for interfacing it to the memory **[Figure 1, #22**

& Column 4, Lines 1-12]; a second bus interface coupled to a second one of the plurality of agents **[Figure 1, #10b]** for interfacing it to the memory **[Column 4, Lines 1-12]**; wherein said first and second bus interfaces comprise: request logic for submitting requests; snoop logic, for responding to snoops; and response logic, for receiving requested data **[Column 5, Lines 6-51]**; and a memory controller coupled to the memory **[Figure 1, #24, Figure 2A, # 27]**, said memory controller receiving requests from said first and second agents, and for globally ordering said requests; wherein responses to said requests are latency independent **[Column 2, Lines 17-28 & Column 6, Lines 16-27]**.

b. **As per Claim 2,** Carpenter discloses the system-on-a-chip as recited in claim 1 wherein the plurality of agents comprise microprocessor cores **[Figure 1, #12a-12d]**.

c. **As per Claim 3,** Carpenter discloses the system-on-a-chip as recited in claim 2 wherein each of said microprocessor cores include a cache **[Figure 1, #14a-14d]**.

d. **As per Claim 4,** Carpenter discloses the system-on-a-chip as recited in claim 1 wherein said first and second bus interfaces and said memory controller are coupled to a common bus **[Column 4, Line 65 – Column 5, Line 5]**.

e. **As per Claim 5,** Carpenter discloses the system-on-a-chip as recited in claim 1 wherein said first and second bus interfaces and said memory controller are coupled to disparate buses **[Column 4, Line 65 – Column 5, Line 5 & Column 5, Lines 52-67]**.

f. **As per Claim 6,** Carpenter discloses the system-on-a-chip as recited in claim 1 wherein said first and second bus interfaces provide coherency between caches within the first and second plurality of agents and the memory **[Column 4, Lines 22-64]**.

g. **As per Claim 7,** Carpenter discloses the system-on-a-chip as recited in claim 1 wherein said request logic submits read and write requests to the memory **[Column 8, Lines 25-56]**.

h. **As per Claim 8,** Carpenter discloses the system-on-a-chip as recited in claim 1 wherein said snoop logic monitors read and write requests to determine whether another one of the plurality of agents requests data that is within its agent **[Figure 2C, #50 & Column 8, Line 66 – Column 9, Line 7]**.

i. **As per Claim 9,** Carpenter discloses the system-on-a-chip as recited in claim 8 wherein if said snoop logic determines that another one of the plurality of agents requests data that is within its agent, said snoop logic informs said memory controller **[Column 5, Lines 20-26]**.

j. **As per Claim 10,** Carpenter discloses the system-on-a-chip as recited in claim 1 wherein said response logic associates received requested data with requests from its agent **[Column 8, Lines 25-56]**.

k. **As per Claim 11,** Carpenter discloses a microprocessor based system comprising: a first microprocessor having a cache for caching data from a memory **[Figure 1, #10a]**, said first microprocessor having a bus interface that implements a plurality of bus phases for a memory transaction **[Column 3, Lines**

38-48 & Column 4, Lines 1-12]; a second microprocessor having a cache for caching data from said memory, said second microprocessor having a bus interface that implements a plurality of bus phases for a memory transaction **[Figure 1, #10b]**; a memory controller, coupled to said memory **[Figure 1, #20 & #24]**; and a global arbiter, coupled to said bus interface of said first microprocessor, to said bus interface of said second microprocessor, and to said memory controller **[Figure 2A, # 27]**, said global arbiter for receiving requests for memory transactions from said first and second microprocessors **[Figure 2A, #12a-#12d]**, and for globally ordering said requests during request phases of said plurality of bus phases, and for initiating snoop phases to said bus interfaces to insure coherency **[Column 2, Lines 40-60, Column 5, Lines 6-51]**, said snoop phases conforming to the globally ordering **[Column 6, Lines 16-27]**; wherein said snoop phases are latency independent with respect to said request phases **[Column 2, Lines 17-28]**.

l. **As per Claim 12,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said plurality of bus phases implemented by said bus interfaces comprise: a request phase, where memory requests are produced by said bus interfaces; a snoop phase, where requests produced by said bus interfaces are observed and responded to; and a response phase, where data associated with a request is received **[Column 5, Lines 6-51]**.

m. **As per Claim 13,** Carpenter discloses the microprocessor based system as recited in claim 12 wherein said memory requests comprise: a request to share;

a request to own; and a write back **[Column 4, Lines 45-64, Column 8, Line 66 - Column 9, Line 7 & Column 9, Table VI]**.

n. **As per Claim 14,** Carpenter discloses the microprocessor based system as recited in claim 13 wherein said request to share results from a read miss in a cache **["Shared" Meaning of Column 9, Table VI]**.

o. **As per Claim 15,** Carpenter discloses the microprocessor based system as recited in claim 13 wherein said request to own results from a write miss in a cache **["Modified" Meaning of Column 9, Table VI]**.

p. **As per Claim 16,** Carpenter discloses the microprocessor based system as recited in claim 13 wherein said write back results from a snoop to a modified cache line **["Pending-modified" Meaning of Column 9, Table VI]**.

q. **As per Claim 17,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said first microprocessor's bus interface comprises: request logic for submitting requests to said memory controller; snoop logic, for observing requests by said second microprocessor; and response logic, for receiving responses to requests submitted by said request logic **[Column 5, Lines 6-51]**.

r. **As per Claim 18,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said first microprocessor's bus interface couples said first microprocessor to a first bus **[Figure 1, #22]**.

s. **As per Claim 19,** Carpenter discloses the microprocessor based system as recited in claim 18 wherein said second microprocessor's bus interface couples said second microprocessor to a second bus **[Figure 1, #22]**.

t. **As per Claim 20,** Carpenter discloses the microprocessor based system as recited in claim 19 wherein said first bus and said second bus are the same **[Column 4, Line 65 – Column 5, Line 5]**.

u. **As per Claim 21,** Carpenter discloses the microprocessor based system as recited in claim 19 wherein said first bus and said second bus are different **[Column 4, Line 65 – Column 5, Line 5 & Column 5, Lines 52-67]**.

v. **As per Claim 22,** Carpenter discloses the microprocessor based system as recited in claim 19 wherein said first bus and said second bus have different timing latencies **[Column 6, Lines 16-27]**.

w. **As per Claim 23,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said memory controller comprises: a bus interface for coupling to said global arbiter **[Figure 2A, #26]**.

x. **As per Claim 24,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said global arbiter comprises a bus interface for coupling to each of said first and second microprocessors and said memory controller **[Figure 2A, #22]**.

y. **As per Claim 25,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said global arbiter comprises a first bus interface for coupling to said first microprocessor, a second bus interface for coupling to said

second microprocessor, and a third bus interface for coupling to said memory controller **[Column 5, Lines 52-67]**.

z. **As per Claim 26,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said global arbiter comprises: a plurality of request queues; a plurality of snoop queues; and a plurality of response queues; wherein each of said queues stores a plurality of requests, snoops, and responses, respectively **[Column 5, Lines 6-51 & Column 3, Lines 38-48]**.

aa. **As per Claim 27,** Carpenter discloses the microprocessor based system as recited in claim 11 wherein said global arbiter comprises: ordering and arbitration logic for receiving a plurality of requests from said first and second microprocessors **[Figure 1, #14a-14d]**, and for ordering said plurality of requests into a global order **[Column 6, Lines 16-27]**.

bb. **As per Claim 28,** Carpenter discloses the microprocessor based system as recited in claim 27 wherein said ordering and arbitration logic initiates snoops according to said global order **[Column 2, Lines 17-28 & Column 6, Lines 16-27]**.

cc. **As per Claim 29,** Carpenter discloses the microprocessor based system as recited in claim 28 wherein said snoops have differing latencies depending on bus characteristics of busses coupling said global arbiter to said first and second microprocessors **[Column 1, Lines 56-67 & Column 6, Lines 16-27]**.

dd. **As per Claim 30,** Carpenter discloses a global arbiter for use in processor based system to insure coherency between a memory and a plurality of agents **[Figure**

2A, #27], the global arbiter comprising: request logic, for receiving requests from each of the plurality of agents; snoop logic, for initiating snoops to the plurality of agents; and ordering logic, coupled to said request logic and said snoop logic, for establishing a global order for said requests, and for insuring that said initiated snoops conform to said global order; wherein said initiated snoops are latency independent with respect to said requests **[Column 5, Lines 6-51 & Column 2, Lines 17-28]**.

ee. **As per Claim 31,** Carpenter discloses the global arbiter as recited in claim 30 wherein said plurality of agents comprise: processor cores; and I/O devices **[Figure 1, #10a & #10b]**.

ff. **As per Claim 32,** Carpenter discloses the global arbiter as recited in claim 31 wherein said processor cores each have a cache **[Figure 1, #14a-14d]**.

gg. **As per Claim 33,** Carpenter discloses the global arbiter as recited in claim 30 wherein said request logic comprises a plurality of queues for receiving said requests from the plurality of agents and for presenting said requests to said ordering logic **[Column 3, Lines 38-48]**.

hh. **As per Claim 34,** Carpenter discloses the global arbiter as recited in claim 30 wherein said snoop logic comprises a plurality of queues for storing snoops conforming to said global order **[Column 8, Line 66 - Column 9]**.

ii. **As per Claim 35,** Carpenter discloses the global arbiter as recited in claim 30 wherein said ordering logic causes said snoop logic to initiate snoops according to said global order **[Column 2, Lines 17-28 & Column 6, Lines 16-27]**.

jj. **As per Claim 36,** Carpenter discloses the global arbiter as recited in claim 30 wherein said global order is established according to a first-in first-out rule **[Column 2, Lines 40-60, Column 5, Lines 6-51 & Column 6, Lines 16-27]**. *Examiner understands that using a transaction queue inherently involves a FIFO arrangement.*

kk. **As per Claim 37,** Carpenter discloses the global arbiter as recited in claim 30 wherein said ordering logic insures that responses to said requests are performed according to said global order **[Column 2, Lines 40-60, Column 5, Lines 6-51 & Column 6, Lines 16-27]**.

ll. **As per Claim 38,** Carpenter discloses the global arbiter as recited in claim 30 further comprising: response logic for insuring that responses to said requests are performed according to said global order **[Column 2, Lines 40-60, Column 5, Lines 6-51 & Column 6, Lines 16-27]**.

mm. **As per Claim 39,** Carpenter discloses the global arbiter as recited in claim 30 further comprising: a plurality of bus interfaces for coupling said global arbiter to the plurality of agents **[Column 1, Lines 56-67 & Column 6, Lines 16-27]**.

nn. **As per Claim 40,** Carpenter discloses the global arbiter as recited in claim 39 wherein at least one of said plurality of bus interfaces couples to a bus that is different than the others **[Column 4, Line 65 – Column 5, Line 5 & Column 5, Lines 52-67]**.

oo. **As per Claim 41,** Carpenter discloses the global arbiter as recited in claim 39 wherein at least one of said plurality of bus interfaces couples to a bus that supports a plurality of virtual channels **[Column 5, Lines 52-67]**.

pp. **As per Claim 43,** Carpenter discloses a multiphase protocol for insuring coherency between agents that share a memory through disparate fabrics, the protocol comprising: a request phase, where memory requests are presented to a global arbiter, said global arbiter ordering said memory requests into a global order **[Column 2, Lines 40-60 & Column 6, Lines 16-27]**; a snoop phase, where snoops are presented to agents coupled to the disparate fabrics according to said global order; and a response phase, where responses to said memory requests are provided according to said global order upon completion of their associated snoops **[Column 3, Lines 38-48, Column 5, Lines 6-51 & Column 6, Lines 16-27]**.

qq. **As per Claim 44,** Carpenter discloses the multiphase protocol as recited in claim 43 wherein the agents comprise a plurality of processor cores **[Figure 1, #12a-12d]**.

rr. **As per Claim 45,** Carpenter discloses the multiphase protocol as recited in claim 44 wherein each of the agents further comprise a cache **[Figure 1, #14a-14d].**

ss. **As per Claim 46,** Carpenter discloses the multiphase protocol as recited in claim 43 wherein the disparate fabrics comprise a plurality of interfaces **[Figure 1, #20]**.

tt. **As per Claim 47,** Carpenter discloses the multiphase protocol as recited in claim 46 wherein at least one of said plurality of interfaces comprises a bus **[Figure 1, #22]**.

uu. **As per Claim 48,** Carpenter discloses the multiphase protocol as recited in claim 43 wherein at least one of said plurality of interfaces comprises a serial fabric **[Column 12, Lines 46-59]**.

vv. **As per Claim 50,** Carpenter discloses the multiphase protocol as recited in claim 43 wherein said request phase, said snoop phase, and said response phase pertains to each of said memory requests **[Column 5, Lines 6-51]**.

ww. **As per Claim 51,** Carpenter discloses the multiphase protocol as recited in claim 50 wherein said request, snoop, and response phases for one of said memory requests may overlap with said request, snoop, and response phases for another one of said memory requests **[Column 6, Lines 16-27]**.

xx. **As per Claim 52,** Carpenter discloses the multiphase protocol as recited in claim 43 wherein said memory requests comprise: memory reads; and memory writes **[Column 8, Lines 25-56]**. *Examiner understands that "data send" and "data receive" inherently include reading and writing to memory.*

yy. **As per Claim 53,** Carpenter discloses a method for providing latency independent coherence among a plurality of agents that share a memory, the method comprising: establishing three phases for memory requests comprising: a request phase; a snoop phase; and a response phase **[Column 5, Lines 6-51]**; when multiple memory requests are outstanding, establishing a global order for

the requests, each of the requests submitted during the request phase **[Column 2, Lines 40-60 & Column 6, Lines 16-27]**; entering a snoop phase for each of the requests, following its request phase, the snoop phase querying the plurality of agents to determine whether they contain data pertaining to the requests **[Column 5, Lines 6-51]**; and entering a response phase for each request after the plurality of agents have responded to the snoop phase for the request, the response phase providing data pertaining to the request to its requesting agent **[Column 5, Lines 6-51]**.

zz. **As per Claim 54,** Carpenter discloses the method as recited in claim 53 wherein the request phase comprises submitting a request from an agent to a global arbiter **[Column 5, Lines 52-67]**.

aaa. **As per Claim 55,** Carpenter discloses the method as recited in claim 54 wherein the request phase further comprises receiving the request by the global arbiter, and ordering the request according to the global order **[Column 2, Lines 40-60 & Column 6, Lines 16-27]**.

bbb. **As per Claim 56,** Carpenter discloses the method as recited in claim 53 wherein the snoop phase comprises communicating requests to the agents that share the memory according to the global order **[Column 2, Lines 40-60 & Column 5, Line 52 – Column 6, Line 27]**.

ccc. **As per Claim 57,** Carpenter discloses the method as recited in claim 56 wherein the snoop phase further comprises awaiting a snoop response from the agents before proceeding to the response phase **[Column 7, Lines 48-60]**.

ddd. **As per Claim 58,** Carpenter discloses the method as recited in claim 53 wherein the response phase comprises providing data associated with a request to the agent that generated the request, according to the global order **[Column 2, Lines 40-60 & Column 6, Lines 16-27]**.

eee. **As per Claim 59,** Carpenter discloses the method as recited in claim 53 wherein the global order causes response phases associated with each request to be completed, in order, without regard to latencies between memory requests **[Column 2, Lines 40-60 & Column 6, Lines 16-27]**.

fff. **As per Claim 60,** Carpenter discloses the method as recited in claim 53 wherein the global order causes response phases associated with each request to be completed, in order, without regard to latencies between a global arbiter and its agents **[Column 6, Lines 16-27]**.

ggg. **As per Claim 61,** Carpenter discloses a computer program product for use with a computing device, the computer program product comprising: a computer usable medium, having computer readable program code embodied in said medium, for causing a system-on-a-chip, having processor cores each having a cache and sharing a memory, to be described, said computer readable program code comprising: first program code for providing a global arbiter, coupled to each of the processor cores **[Column 4, Lines 1-12 & Column 5, Lines 6-51]**; and second program code for providing a bus interface for each of the processor cores to couple the processor cores to the global arbiter **[Figure 2A, #26]**; third program code for providing a bus interface to couple the global arbiter to the

memory **[Column 5, Lines 6-51]**; wherein said global arbiter receives memory requests from each of the processor cores, establishes a global order for the requests, and initiates a snoop phase for each of the requests according to the global order; and wherein the processor cores respond to the snoop phase initiated by the global arbiter at different times **[Column 2, Lines 40-60 & Column 8, Line 25 – Column 9, Line 7]**.

hhh. **As per Claim 62,** Carpenter discloses the computer program code product as recited in claim 61 wherein the global arbiter comprises: request logic, for receiving requests from the processor cores; snoop logic, for communicating received requests from the global arbiter to the processor cores; and ordering logic, for establishing a global order for received requests, and for causing said snoop logic to communicate the received requests to the processor cores according to the global order **[Column 5, Lines 6-51]**.

iii. **As per Claim 63,** Carpenter discloses the computer program code product as recited in claim 62 wherein the global arbiter further comprises: response logic, for causing responses to the received requests to be provided upon completion of their associated snoop **[Column 5, Lines 6-51]**.

jjj. **As per Claim 64,** Carpenter discloses the computer program code product as recited in claim 62 wherein the global arbiter further comprises: response logic, for causing responses to the received requests to be provided to the processor cores according to the global order **[Column 5, Lines 6-51 & Column 6, Lines 16-27]**.

kkk. **As per Claim 65,** Carpenter discloses a computer data signal embodied in a transmission medium comprising: computer-readable program code for providing a latency independent coherence protocol, said program code comprising: first program code for providing a request phase for a memory request to be transmitted from an agent to a global arbiter; second program code for providing a snoop phase where the memory request is ordered by said global arbiter according to a global order, and transmitted to other agents according to said global order; and third program code for providing a response phase where the response to said memory request is provided to said agent, upon completion of said snoop phase **[Column 2, Lines 40-60, Column 4, Lines 1-12 & Column 5, Lines 6-51]**; wherein by establishing a global order for memory requests, a memory is shared by a plurality of agents that are connected to said global arbiter by fabrics having different latencies **[Column 6, Lines 16-27]**.

lll. **As per Claim 66,** Carpenter discloses the computer data signal as recited in claim 65 wherein said global arbiter comprises: a plurality of bus interfaces, one for each of said fabrics **[Figure 1, #22]**; request logic, coupled to said plurality of bus interfaces, for receiving said memory request; ordering logic, coupled to said request logic, for receiving said memory request from said request logic, and for establishing said global order upon receipt; and snoop logic, coupled to said ordering logic, for submitting snoop requests to said other agents according to said global order **[Column 2, Lines 40-60, Column 5, Lines 6-51 & Column 6, Lines 16-27]**.

mmm. **As per Claim 67,** Carpenter discloses the computer data signal as recited in claim 66 further comprising: response logic, for providing a response to said memory request when said snoop requests are completed **[Column 2, Lines 40-60, Column 5, Lines 6-51 & Column 6, Lines 16-27]**.

nnn. **As per Claim 68,** Carpenter discloses the computer data signal as recited in claim 67 wherein said snoop requests are completed when each of said other agents have responded to said global arbiter **[Column 2, Lines 40-60, Column 5, Lines 6-51 & Column 7, Lines 48-60]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 42 & 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al. (US Patent # 6,067,611) as applied to claims 30-41 & 43-48 above, and further in view of Mowery et al. (US Patent # 6,898,766), herein **Carpenter** and **Mowery**, respectively.

a. **Carpenter** does not expressly disclose a PCI-Express bus interface.

b. **As per Claim 42, Mowery** discloses the global arbiter as recited in claim 41 wherein said at least one of said plurality of bus interfaces comprises a bus interface to PCI-Express **[Column 4, Lines 4-22]**.

c. **As per Claim 49, Mowery** discloses the multiphase protocol as recited in claim 48 wherein said serial fabric comprises PCI-Express **[Column 4, Lines 4-22]**.

d. **Carpenter** and **Mowery** are analogous art because they are from a similar problem solving area: communication interfaces of integrated circuits. At the time of invention, it would have been obvious for one of ordinary skill in the art to combine the bus interfaces, as taught by **Carpenter**, with the PCI-Express interface, as taught by **Mowery**. The suggestion/motivation for doing so would have been to reduce engineering time and costs associated with designing a new computer interface as disclosed by **Mowery [Column 2, Lines 5-8]**.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nunez et al. (US Patent # 6,275,906) teaches a coherency scheme for a memory subsystem. Borrill et al. (US Patent # 5,588,131) teaches snooping and snarfing within a multiprocessor, remote memory system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabahn can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMM

Mano Padmanabhan
5/12/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER